**ABSTRACT**

A DRAM array is provided capable of being interchanged between single-cell and twin-cell array operation for storing data in a single-cell or a twin-cell array format, respectively. Preferably, the DRAM array is operated in the single-cell array format during one operating mode and the DRAM array is operated in the twin-cell array format during another operating mode. Wordline decoding circuitry is included for interchanging the DRAM array between single-cell and twin-cell array operation. The wordline decoding circuitry includes a pre-decoder circuit for receiving a control signal and outputting logic outputs to wordline activation circuitry. The wordline activation circuitry then activates at least one wordline traversing the array for interchanging memory cells within the DRAM array between single-cell array operation and twin-cell array operation. Methods are also provided for converting data stored within the DRAM array from the single-cell to the twin-cell array format, and vice versa.

10512018.020901